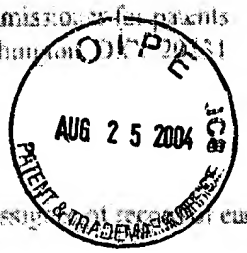
Commissioner for patents
Washington, D.C. 20231



POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST
(REVOCATION OF PRIOR POWERS)

As assignee of record of each of the patent applications listed in the table of attachment A,

REVOCATION OF PRIOR POWERS OF ATTORNEY

all powers of attorney previously given in each of the listed patent applications are hereby revoked, and

NEW POWER OF ATTORNEY

The following attorneys/agents are hereby appointed to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith. I hereby appoint all attorneys of Thomas, Kayden, Horstemeyer & Risley, LLP, who are listed under the USPTO Customer Number shown below as the attorneys to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith, recognizing that the specific attorneys listed under that Customer Number may be changed from time to time at the sole discretion of Thomas, Kayden, Horstemeyer & Risley, LLP, and request that all correspondence about the application be addressed to the address filed under the same USPTO Customer Number.

24504
Patent Trademark Office

Please direct all future correspondence and telephone calls to:

Daniel R. McClure, Reg. No. 38,962
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.
100 Galleria Parkway, Suite 1750
Atlanta, Georgia 30339
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ASSIGNEE OF ENTIRE INTEREST

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.
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Hsinchu, Taiwan 300-77, R.O.C.

ASSIGNEE CERTIFICATION

The certification under 37 C.F.R. §3.73(b) establishing the right of assignee to take action is attached hereto along with documentation evidencing same. Further, in my official position with Taiwan Semiconductor Manufacturing Company, Ltd., I am authorized to sign documents and otherwise act on its behalf in connection with the management and handling of patent applications and other intellectual property matters.

Date May 24, 2004

Chien-Wei (Chris) Chou
Director - Intellectual Property Division

No	Serial No	TSMC No.	Application Title	Filing Date	Assignment (Reel/Frame)
1	10/120,834	TS1999705C	Process For High Voltage Oxide And Select Gate Poly For Split-Gate Flash Memory	4/11/2002	012791/0621
2	10/074,882	TS2000885	Methodology To Reduce The Early Failure Rate By Applying Dynamic Voltage Stressing In Testing With Screen Criteria Of Delta LSB	2/12/2002	012599/0107
3	09/933,961	TS20010325	Electrostatic Discharge-Free Container For Insulating Articles	8/22/2001	012128/0489
4	10/058,473	TS20011063	Enhanced Adhesion Strength Between Mold Resin And Polyimide	1/28/2002	014216/0356
5	10/040,233	TS20010102	Novel Design And Fabrication Method For Finger N-Type Doped Photodiodes With High Sensitivity For CIS Products	11/7/2001	Filed 3-29-04 Copy attached
6	10/225,803	TS20010389	HDP Gap-Filling Process For Structures With Extra Step At Side-Wall	8/22/2002	013228/0267
7	10/679,737	TS20011380B	Method For Forming A Novel Top-Metal Fuse Structure	10/6/2003	012593/0150
8	10/437,092	TS20010996B	Horizontal Surrounding Gate MOSFETS	5/13/2003	013308/0785
9	10/338,138	TS20011442	Integrated High Performance MOS Tunneling Led In ULSI Technology	1/8/2003	013647/0832
10	10/177,912	TS20011051	Structure And Method For Low-Stress Concentration Solder Bumps	6/20/2002	013041/0230
11	10/313,501	TS20011509	Multivariate RBR Tool Aging Detector	12/6/2002	Copy attached
12	09/932,680	TS1998850/852BCC	Tilt-Angle Ion Implant To Improve Junction Breakdown In Flash Memory Application	8/20/2001	010367/0646
13	09/905,408	TS20010133	Selective Formation Of Metal Gate For Dual Fate Oxide Application	7/16/2001	012011/0342
14	10/288,194	TS20020083	Self-Aligned Structure With Unique Erasing Gate In Split Gate Flash	11/8/2002	013483/0576
15	10/255,482	TS20020058	Method To Prevent Side Lobe On Seal Ring	9/26/2002	013341/0450
16	10/245,433	TS20011294	Metal Fuse For semiconductor devices	9/17/2002	

Date: May 24, 2004